IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application: T. SAKATA et al

Serial No. 09/349,761 Filed: July 9, 1999

Group Art Unit: 2133

Examiner: J. Torres

For: SEMICONDUCTOR INTEGRATED CIRCUIT WITH MEMORY REDUNDANCY CIRCUIT

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner of Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, the applicants inform the Examiner of the documents cited during prosecution of the parent application, Serial No. 09/349,761.

The above-referenced patent application is a continuation application of U.S. Serial No. 09/349,761, filed July 9, 1999, from which priority is claimed under 35 U.S.C. § 120.

Applicants request the Examiner to initial and return a copy of the attached PTO-1449 form to indicate that the references have been considered.

Respectfully/submitted,

Registration No. 30,293 Attorney for Applicant(s)

MATTINGLY, STANGER & MALUR 1800 Diagonal Road, Suite 370 Alexandria, Virginia 22314 (703) 684-1120

Date: June 23, 2003

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